Investigation of Material and Geometric Effects on the Performance of Gate All Around Nanowire TFET and FET Devices

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Abstract. Advancements in nanoscale technology have enabled lower operating voltages and reduced power consumption, but also increased leakage currents. This study explores the performance of Tunnel Field-Effect Transistors (TFETs) and Field-Effect Transistors (FETs) using gate-all-around (GAA) silicon nanowires (Si-NW), which offer improvements over traditional MOSFETs by reducing short channel effects. The optimized GAA NWTFETs achieved a significant reduction in threshold voltage (69.5%) and leakage current (6.39%), while enhancing ON current, subthreshold swing, and ON/OFF current ratio. Similarly, the optimized GAA NWFETs demonstrated a substantial reduction in leakage current (97.59%) and a dramatic improvement in the ON/OFF current ratio by 4611.97%. These results highlight the potential of GAA nanowire TFETs and FETs in advancing semiconductor technologies with improved performance and energy efficiency.

Keywords: Gate-All-Around (GAA); Tunnel Field-Effect Transistor (TFET); Field-Effect Transistor (FET); Silicon Nanowire (Si-NW).

1. Introduction

In recent years, Tunnel Field Effect Transistors (TFETs) have emerged as promising alternatives to traditional MOSFETs, particularly as device dimensions continue to scale down. TFETs offer significant advantages over MOSFETs, such as mitigating Short Channel Effects (SCE), reducing OFF currents (IOFF), and achieving smaller subthreshold swings (SS) [1-3]. However, a notable drawback of TFETs is their relatively low ON current (ION), which limits their overall performance. To address this challenge, transitioning it to a Gate All Around (GAA) structure promises to improve both IOFF and the ION/IOFF current ratio by providing superior gate coupling and operational efficiency. Similarly, Gate All Around Field Effect Transistors (GAAFETs) have demonstrated superior gate control and performance due to their ability to uniformly spread electric field lines around a symmetrical channel, avoiding the corner effects seen in square channel designs [4-6]. This leads to better control over short channel effects and reduced off currents. To optimize GAAFET structures, it is crucial to compare the performance of square and cylindrical channels, focusing on gate control, short channel effects, and off currents.

This study aims to optimize both GAA TFETs and GAA FETs in terms of their current ratio (ION/IOFF), leakage current (IOFF), and ON current (ION). By conducting 2D and 3D simulations and comparative analyses, this research seeks to enhance the design and performance of these advanced transistors, paving the way for more efficient and powerful electronic devices.

2. Methodology

2.1. Modelling of Si-NW GAA TFET

The Silvaco TCAD simulator is utilized to model and simulate a Silicon Nanowire Gate-All-Around Tunneling Field-Effect Transistor (Si-NW GAA TFET). The process simulator, Athena, is used for designing the device structure, while Atlas simulates the electrical behavior, analyzing DC, AC, and time domain responses based on either 2D or 3D structures. Deckbuild serves as the runtime environment for these simulations, and Tonyplot is used to visualize and analyze the resulting data.
The device modeling focuses on an n-type TFET (nTFET), which requires positive gate and drain voltages to activate. The cylindrical GAA structure, achieved through a specialized mesh configuration, provides superior control over current flow compared to other transistor designs. Specific models, such as non-local tunneling, Shockley-Read-Hall recombination, Auger recombination, and others, are employed to accurately simulate the TFET behavior. Subsequent to the defining of materials and contacts within Atlas, the simulation is conducted, and results are visualized using Tonyplot. Key geometrical and material parameters used in the simulation include channel length, channel radius, oxide thickness, gate metal workfunction, dielectric constant, and drain voltage, all of which play crucial roles in determining the device's performance.

2.2. Modelling of Si-NW GAA FET

Similar to the Si-NW GAA TFET, the Silvaco TCAD tool was used to simulate a 3D Si-NW GAA FET, with Atlas simulating its electrical behavior. Tonyplot was chosen for graph plotting, particularly the Id-Vg characteristics for further analysis. In the device modeling, a Constant Voltage and Temperature method was employed to simulate the GAA NWFET, integrating various mobility models, including field-dependent, phonon scattering, impurity scattering, and surface roughness-induced mobility. The Shockley–Read–Hall (SRH) model was used to analyze recombination effects, along with the Auger recombination model, which describes electron-hole recombination with energy release. The Newton-Gummel method was utilized to improve the accuracy of the simulation, starting with decoupled iterations and transitioning to Newton iterations if needed. This approach provided a deeper understanding of the carrier transport in GAA FETs and offered insights for optimizing device performance.

2.3. Analysis of parameters

In this study, the performance of Si-NW GAA TFET ans Si-NW GAA FET will be analyzed by extracting and evaluating several key parameters through simulations conducted using the Silvaco TCAD tool. The threshold voltage (Vth) will be determined using the Constant Current (CC) method, chosen for its simplicity despite its reliance on user-defined values that may introduce variability. The ON/OFF current ratio (Ion/Ioff) will be analyzed by examining the Id-Vg characteristic graph, with a focus on achieving a high Ion, low Ioff, and an optimal ON/OFF ratio, which are crucial for high-voltage applications. The subthreshold slope and subthreshold swing will be calculated from the linear region of the Id-Vg curve in the subthreshold region, aiming for a subthreshold swing below 60mV/decade, indicative of superior

performance due to the band-to-band tunneling mechanism in TFETs. Additionally, Drain Induced Barrier Lowering (DIBL) will be assessed by comparing threshold voltages at different drain voltages, providing insights into the transistor's behavior and its susceptibility to drain voltage variations, particularly important for nanoscale devices.

3. Results and discussion

3.1. Silicon nanowire GAA TFET

The simulation results from the base case of the Si-NW GAA TFET serve as a benchmark for comparison with optimized designs. The base case parameters, including a gate length of 200 nm, channel radius of 40 nm, and oxide thickness of 4 nm, are detailed in the analysis. Using the constant current method, the threshold voltage is determined to be 0.2654V. The leakage current is found to be 1.2884×10^{-10} A, while the current at the saturated region reaches 1.5028×10^{-4} A. From these values, the ON/OFF current ratio is calculated as 1.1664×10^{6}, indicating the switching efficiency of the device. Additionally, the subthreshold swing (SS) is measured at 23.84 mV/decade, and the drain-induced barrier lowering (DIBL) is calculated to be 27.35 mV/V. These results suggest that while the base case provides a solid foundation, there is still room for optimization to improve the device's performance, particularly in reducing the SS and DIBL values. Hence, a few parameters have been studies throughout this study towards the device.
In this study, the performance of the Si-NW GAA TFET was analyzed by varying key parameters such as channel radius, oxide thickness, gate metal workfunction, dielectric constant, and channel length. Each of these parameters was systematically adjusted to evaluate their influence on device behavior. The results, summarized in the following tables, provide insights into how these variations affect critical performance metrics such as threshold voltage, ON/OFF current ratio, subthreshold swing, and DIBL.

Table 1. Summarized Results for Different Channel Length

Performances	Channel Length (nm)		
	100	**150**	**200**
V_{th}	0.2611	0.2650	0.2653
I_{off}	7.1644E-18	9.70004E-18	1.2884E-17
I_{on}	1.5258E-5	1.5277E-5	1.5028E-5
$\frac{I_{on}}{I_{off}}$	2.1277E12	1.57450E12	1.1664E12
SS	30.74	27.02	27.94
DIBL	26.8696	28.7826	27.3913

Table 2. Summarized Results for Different Channel Radius

Performances	Channel Radius (nm)			
	10	**20**	**30**	**40**
V_{th}	0.1448	0.2290	0.2400	0.2653
I_{off}	2.0867E-18	4.5998E-18	8.4057E-18	1.2884E-17
I_{on}	1.0646E-6	6.0837E-6	1.2166E-5	1.5028E-5
$\frac{I_{on}}{I_{off}}$	5.1028E11	1.3226E12	1.4474E12	1.1664E12
SS	23.19	22.19	23.89	23.84
DIBL	62.3478	36.0870	33.6522	27.3913

Table 3. Summarized Results for Different Oxide Thickness

Performances	Channel Radius (nm)			
	2	**3**	**4**	**5**
V_{th}	0.0956	0.1677	0.2654	0.3452
I_{off}	1.3493E-17	1.3136E-17	1.2884E-17	1.2636E-17
I_{on}	2.7730E-5	2.1097E-5	1.5028E-5	9.9659E-6
$\frac{I_{on}}{I_{off}}$	2.0552E12	1.6061E12	1.1264E12	8.0630E11
SS	16.44	18.53	22.18	27.39
DIBL	10.52	29.04	27.30	51.07

Table 4. Summarized Results for Different Gate Metal Workfunction

Performances	Gate Metal Work Function (eV)			
	4.0 (Silicon)	**4.4 (Silver)**	**4.6 (Copper)**	**4.8 (Tungsten)**
V_{th}	0.2968	0.5653	0.7653	0.9653
I_{off}	1.2884E-17	1.2628E-17	1.1307E-17	7.1368E-18
I_{on}	1.5028E-5	5.2638E-6	1.6208E-6	3.0519E-7
$\frac{I_{on}}{I_{off}}$	1.1664E12	4.1682E11	1.4334E11	4.2763E10
SS	23.84	23.87	23.87	23.87
DIBL	27.74	27.39	27.39	27.39

Table 5. Summarized Results for Different Oxide Dielectric Constant

Performances	Oxide Dielectric Constant			
	7.5 (Si_3N_4)	**10 (Al_2O_3)**	**22 (ZrO_2)**	**25 (HfO_2)**
V_{th}	0.9304	0.7330	0.3090	0.2653
I_{off}	1.0411E-17	1.1175E-17	1.2624E-17	1.2884E-17
I_{on}	1.2405E-8	2.6720E-7	1.1708E-5	1.4028E-5
$\frac{I_{on}}{I_{off}}$	1.1915E9	2.3909E10	9.2742E11	1.1664E12
SS	52.60	45.91	29.03	23.84
DIBL	224.87	115.65	33.74	27.39

Based on the simulation results, the optimal values for channel radius, oxide thickness, gate metal workfunction, dielectric constant, and channel length were selected for further optimization of the Si-NW GAA TFET device. These parameters, which demonstrated the best performance during the initial analysis, have been combined to enhance the overall efficiency and functionality of the device [7-8]. The optimized parameters are presented in the table below.

Table 6. Optimized Parameters for the device

Parameters	This Work
Gate Length	150nm
Channel Radius	30nm
Oxide Thickness	2nm
Source Length	80nm
Drain Length	80nm
Oxide Dielectric Constant	25
Gate Metal Work Function	4eV

Parameters	This Work
P-doping Concentration	1e19 /*cm*-
N-doping Concentration	1e19 /*cm*-
Channel Doping Concentration	1e17 /*cm*-
Drain Voltage	1.2V

Using the constant current method at 1×10^{-12} A, the threshold voltage was found to be 0.0809 V, which represents a 69.5% decrease from the base case. The leakage current was reduced by 6.39% to 1.2060×10^{-17}A, while the on current increased by 0.87%. Importantly, the on off current ratio, a key performance indicator, was successfully increased by 7.77% using the optimized parameters. Another significant achievement of this work is the reduction of the subthreshold swing to 11.63 mV/dec, which is 51.22 mV/dec lower than the base case, indicating a steeper slope. Additionally, the Drain-Induced Barrier Lowering (DIBL) was improved to 8.70 mV/V, compared to 27.35 mV/V in the base case. These improvements highlight the effectiveness of the selected parameters in optimizing the Si-NW GAA TFET device's performance.

3.2. Silicon nanowire GAA FET

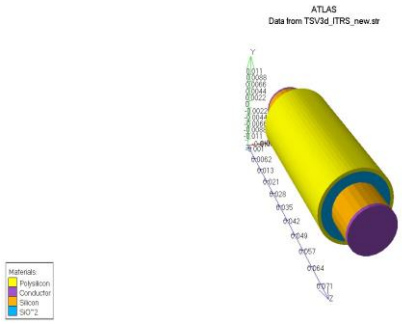

Figure 1. Structure of GAA NW FET

In the 3D model above, it is clearly shown that there are no other conducting materials except silicon which means that the drain current is only allowed to flow through the nanowire [9]. Thus, behavioural characteristics of a silicon nanowire GAA structure can be easily understood.

The 3D model depicted in the figure represents a silicon nanowire Gate-AllAround (GAA) structure, showcasing various materials including polysilicon, a conductor, silicon, and silicon dioxide (SiO_2). In this design, silicon is the sole conducting material, ensuring that the drain current flows exclusively through the nanowire. This setup simplifies the analysis of the silicon nanowire GAA's behavioral characteristics.

The design parameters utilized in this study have been meticulously selected as follows: The channel length is set at 50 nm [10] and the channel radius is 7 nm, based on Lee *et al.* [11]. An oxide thickness of 3 nm is incorporated following a study by Anand *et al.* [12]. The doping concentration is specified as $1e19cm^3$ and the operational temperature is maintained at 300 K.

The design includes a 1 nm thick conductor. Additionally, the gate metal work function values are specified as 4.1 eV and 5.2 eV [13]. These carefully chosen parameters form the foundation for studying the silicon nanowire GAA structure's electrical characteristics and performance.

This study examines the performance of silicon nanowire GAA FETs with three different gate oxide configurations: pure SiO_2, a stack of SiO_2 and HfO_2, and a stack of SiO_2, HfO_2, and TiO_2. The simulation results indicate that the inclusion of high-*k* materials such as HfO_2 and TiO_2 in the gate oxide stack

significantly influences device performance. Specifically, the threshold voltage (Vth) increases with the addition of these high-*k* layers, which enhances gate control but also shifts the threshold voltage higher. For instance, the Vth increases from the SiO_2 configuration to the SiO_2 and HfO_2 stack, and further with the SiO_2, HfO_2, and TiO_2 stack. The results from these different configurations are analysed and the best design is selected for further optimization.

Table 7. Simulation Results of ON/OFF Current Ratio with Different Oxide Configuration

Performances	Oxide Configuration		
	SiO2	**SiO2, HfO2 (stack)**	**SiO2, HfO2, TiO2 (stack)**
I_{off}	4.56374E-12	9.01982E-16	1.2433E-17
I_{on}	4.84882E-6	5.56551E-6	5.66747E-6
$\frac{I_{on}}{I_{off}}$	1.062E6	6.1703E9	4.5584E11

The study found that incorporating high-*k* materials such as HfO_2 and TiO_2 in the gate oxide stack of silicon nanowire GAA FETs significantly enhances device performance. The SiO_2, HfO_2, TiO_2 stack configuration showed the lowest leakage current (Ioff) and the highest on-state current (Ion), resulting in a greatly improved Ion/Ioff ratio. This configuration offers superior drive capability with minimal leakage, making it the most effective design for enhancing the overall performance of the device. Hence, this design will be further use for optimization in Silicon Nanowire GAA FET.

Subsequently, the effect of varying oxide thickness, gate length, channel radius and nanowire materials on the performance of silicon nanowire GAA FET with three stack oxide configurations was investigated. The analysis covered key parameters such as threshold voltage, ON/OFF current ratio, leakage current, and subthreshold swing. All the detailed simulation results and performance metrics are summarized in the Tables 8, 9, 10 and 11.

Table 8. Summarized Results for Different Oxide Thickness

Performances	Oxide Thickness (nm)			
	2	**3**	**4**	**5**
V_{th}	0.4066	0.3182	0.3067	0.2020
I_{off}	8.4738E-19	1.2433E-17	3.4838E-17	3.0014E-15
I_{on}	6.4570E-6	5.6675E-6	5.5328E-6	5.0587E-6
$\frac{I_{on}}{I_{off}}$	7.6200E12	4.5584E11	1.5881E11	1.6850E9
SS	60.34	60.72	60.88	63.21

Table 9. Summarized Results for Different Gate Length

Performances	Gate Length (nm)			
	30	**40**	**50**	**60**
V_{th}	0.3017	0.3090	0.3182	0.2020
I_{off}	1.0065E-16	2.33737E-17	1.2433E-17	3.0014E-15
I_{on}	5.2261E-6	5.5396E-6	5.6675E-6	8.2879E-18
$\frac{I_{on}}{I_{off}}$	5.1923E10	2.3700E11	4.5584E11	7.4000E11
SS	60.36	61.29	60.51	60.20

Table 10. Summarized Results for Different Channel Radius

Performances	Oxide Thickness (nm)			
	5	6	7	8
V_{th}	0.5021	0.4092	0.3182	0.2248
I_{off}	2.85562E-21	4.64603E-19	1.2433E-17	4.39367E-16
I_{on}	3.22274E-6	4.34522E-6	5.6675E-6	7.16216E-6
$\frac{I_{on}}{I_{off}}$	1.1285E15	9.3525E12	4.5584E11	1.6301E10
SS	54.85	60.27	60.71	61.54

Table 11. Summarized Results for Different Nanowire Materials

Performances	Nanowire Materials		
	Silicon	Germanium	InP
V_{th}	0.3182	0.6030	0.2051
I_{off}	4.14252E-8	2.57957E-12	8.80817E-8
I_{on}	5.66747E-6	5.14613E-8	8.51854E-6
$\frac{I_{on}}{I_{off}}$	4.5584E11	1.5058E8	5.4647E9
SS	60.72	232.92	60.55

Based on the results, the parameters that demonstrated the best performance were selected for further optimization of the device Table below shows the base case and the optimized case for Silicon Nanowire GAA FET.

Table 12. Base Case and Optimized Case for Silicon Nanowire GAA FET

Parameters	Base Case	Optimized Case
Oxide Thickness	3nm	2nm
Gate Length	50nm	60nm
Channel Radius	7nm	5nm
Nanowire Material	Si	InP

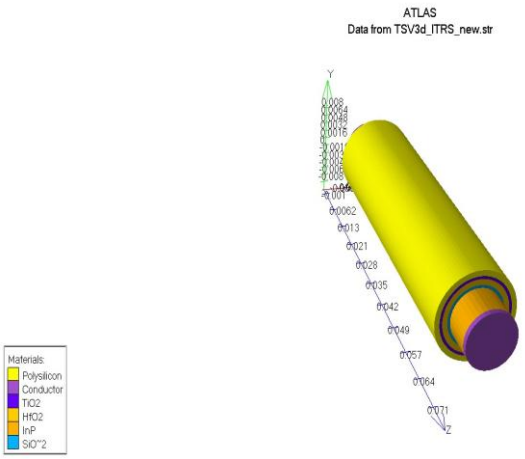

Figure 2. Optimized Silicon Nanowire GAA FET

The optimized design of the nanowire Gate-All-Around (GAA) Field-Effect Transistor (FET) involves several strategic modifications to enhance performance metrics significantly. Firstly, the oxide thickness

is reduced from 3nm to 2nm, which improves gate control over the channel by reducing short-channel effects and minimizing leakage currents. This tighter electrostatic control results in a steeper subthreshold swing, thereby enhancing the transistor's switching characteristics. Secondly, the gate length is extended from 50nm to 60nm, which strengthens the electrostatic control of the gate over the channel. This extension reduces drain-induced barrier lowering (DIBL), leading to an improved threshold voltage and better subthreshold performance.
Thirdly, the channel radius is reduced from 7nm to 5nm. A smaller channel radius increases the gate's control over the channel, further reducing leakage currents and enhancing the ON/OFF current ratio. Lastly, the material of the nanowire is changed from silicon (Si) to indium phosphide (InP), a material known for its higher electron mobility and better performance at nanoscale dimensions. These combined optimizations result in a 27.82% increase in threshold voltage, a 97.59% reduction in leakage current, a 14.88% increase in on current, and an extraordinary 4611.97% improvement in the ON/OFF current ratio, demonstrating a substantial enhancement in the overall efficiency and functionality of the GAA FET. Table 13 will gives a clearer illustration regarding the obtained results.

Table 13. Base Case and Optimized Case for Silicon Nanowire GAA FET

Parameters	Base Case	Optimized Case	Change in Percentage (%)
V_{th}	0.3182	0.40685	+27.82%
I_{off}	1.2433E-17	3.0316E-19	-97.59%
I_{on}	5.66747E-6	6.5121E-6	+14.88%
$\frac{I_{on}}{I_{off}}$	4.5584E11	2.1480E13	+4611.97%

4. Conclusion

The performance of the Silicon Nanowire Gate-All-Around Tunnel Field-Effect Transistors (TFETs) is demonstrated. The impact of various parameters—such as channel length, channel radius, and gate metal work function—on device performance is analyzed to investigate short-channel effects and assess their influence on device characteristics. The device is then optimized, achieving improvements in ON/OFF current ratio, leakage current, and subthreshold swing. The leakage current is reduced by 6.39% and threshold voltage is improved by 69.5%. Subthreshold swing is significantly reduced by 51.22% while current ratio also shows enhancement by increasing 7.77%. DIBL is also improved by 68.2% after the study. Subsequently, the focus shifted to the study and optimization of the Silicon Nanowire Gate-All-Around Field-Effect Transistor (FET). The study aimed to extend the understanding gained from the TFET study and apply it to the FET structure. The Id-Vg transfer characteristic graph was utilized to demonstrate the performance of the GAA FET. Similar to the TFET study, the effects of material and geometrical parameters on the performance of the GAA FET were analyzed. This analysis allowed for the identification of optimal parameter settings that improve the device performance. Through these investigations, the Silicon Nanowire GAA FET was successfully improved and optimized. The leakage current is reduced by 97.59%, ON current is improved by 14.88% and most importantly the current ratio is increased from 4.5584E11 to 2.1480E13 which is improved by 4611.97%. In conclusion, the study led to substantial advancements in the understanding and optimization of both Silicon Nanowire GAA TFET and FET devices. The studies have provided valuable insights into the effects of various parameters and structural modifications on device performance.

References

[1] Rasool, A., Kossar, S., Parveen, S. and Rasool, U., 2024. Heterojunction Tunnel Field-Effect Transistors (TFETs) and Applications. *In Handbook of Emerging Materials for Semiconductor Industry* (pp. 471-479). Singapore: Springer Nature Singapore.

[2] Yau, S.K., Hatta, S.F.W.M., Wahab, Y.A., Aidit, S.N. and Hussin, H., 2022. Process variations and short channel effects analysis in gate-all-around nanowire field-effect transistor using a statistical Taguchi-Pareto ANOVA framework. https://orcid.org/0000-0001-9519-073X

[3] Goh, W.Z., Fong, B., Hussin, H. and Hatta, S.W.M., 2022. Study of Scaling Limits of Multi-Gate Fets (Finfet) With High-*k* Dielectric. *AIJR Proceedings*, pp.123-129.

[4] Qin, L., Li, C., Wei, Y., Hu, G., Chen, J., Li, Y., Du, C., Xu, Z., Wang, X. and He, J., 2023. Recent developments in negative capacitance gate-all-around field effect transistors: a review. *IEEE Access*, 11, pp.14028-14042.

[5] Qin, L., Tian, H., Li, C., Wei, Y., He, J., He, Y., Ren, T., Xu, Z. and Yue, Y., 2024. Double channeled nanotube gate all around field effect transistor with drive current boosted. *Microelectronic Engineering*, 289, p.112171.

[6] Xie, L., Zhu, H., Zhang, Y., Ai, X., Li, J., Wang, G., Liu, J., Du, A., Yang, H., Yin, X. and Huang, W., 2023. Demonstration of germanium vertical gate-all-around field-effect transistors featured by self-aligned high-κ metal gates with record high performance. *ACS nano*, 17(22), pp.22259-22267.

[7] Anand, A., Nair, A.R., Sreekumar, V., Sadasivan, V. and Ramakrishnan, V.N., 2022. SiGe vertical NW GAA TFET with improved current and low leakage. *Materials Today: Proceedings*, 66, pp.1885-1889.

[8] Sreevani, A., Swarnakar, S. and Krishna, S.V., 2022. Comparative study of analog parameters for various silicon-based tunnel field-effect transistors. *Silicon*, 14(15), pp.9223-9235.

[9] Arjmand, T., Legallais, M., Nguyen, T.T.T., Serre, P., Vallejo-Perez, M., Morisot, F., Salem, B. and Ternon, C., 2022. Functional devices from bottom-up Silicon nanowires: A review. *Nanomaterials*, 12(7), p.1043.

[10] Ko, H.L., Luc, Q.H., Huang, P., Wu, J.Y., Chen, S.M., Tran, N.A., Hsu, H.T. and Chang, E.Y., 2022. Sub-10 nm top width nanowire InGaAs gate-all-around MOSFETs with improved subthreshold characteristics and device reliability. *IEEE Journal of the Electron Devices Society*, 10, pp.188-191.

[11] Lee, K.W. and Hong, S.M., 2021. Compact charge model for Si gate-all-around nMOSCAPs with cylindrical cross-sections considering the density-gradient equation. Solid-State Electronics, 181, p.107959.

[12] Reddy, N.N. and Panda, D.K., 2021. Nanowire gate all around-TFET-based biosensor by considering ambipolar transport. *Applied Physics A*, 127(9), p.682.

[13] Kumar, S., Chatterjee, A.K. and Pandey, R., 2021. Performance analysis of gate electrode work function variations in double-gate junctionless FET. *Silicon*, *13*, pp.3447-3459.