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A Low-Voltage High-Speed DRAM Sense Amplifier Employing Hidden Diode-Connected Offset Cancellation

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Abstract. This paper presents a high-speed bit-line sense amplifier (BLSA) designed for low-voltage dynamic random access memory (DRAM). As supply voltages and cell capacitances scale down, BLSA sensing margin is severely degraded by transistor offset and reduced signal levels. While traditional offset-canceling (OC) techniques mitigate these effects, they often introduce additional sensing time. To address this, the proposed architecture utilizes a diode-connected configuration to extract threshold-voltage mismatches, which are subsequently stored in coupling capacitors to compensate offsets. This compensation process is executed simultaneously with charge sharing, effectively hiding the OC timing overhead. Furthermore, a short pre-sensing phase is utilized to enhance the initial sensing margin and accelerate the main sensing operation. Implemented in TSMC 65nm technology, Monte Carlo simulations demonstrate a sensing yield exceeding 99% across a 0.8 V to 1.0 V range. Notably, the design maintains a 100% sensing yield across various process corners and a temperature range of -10°C to 85°C while achieving a fast sensing time of 6.058 ns— which is shorter than those of the compared offset-compensated architectures. With a compact area overhead of 12T+2C, this robust BLSA is highly suitable for sub-1V, low-power memory applications.

Keywords: Bit-Line Sense Amplifier (BLSA), Dynamic Random Access Memory (DRAM), Offset Cancellation (OC), Coupling Capacitor (CC), Sensing Yield

1. Introduction

1.1. The impact of technology node scaling on BLSA performance

The bit-line sense amplifier (BLSA) is a core block for dynamic random access memory (DRAM) to detect and amplify cell value. In a conventional BLSA, the circuit consists of a cross-coupled CMOS latch. When the word-line (WL) is activated, the charge stored in the cell is shared with the bit-line (BL), creating a differential voltage (ΔV) between the BL and its complementary reference bit-line (BLB). The sensing operation then begins by activating the pull-up and pull-down networks, forcing the nodes to the supply voltage (VDD) and ground (GND) based on the initial polarity of ΔV. While technology nodes scale towards sub-10nm (Choe, 2022) to increase chip density, supply voltage (VDD) is also lowered to reduce power consumption. However, this directly weakens the sensing capabilities of BLSA. (Kim et al., 2022; Spessot & Oh, 2020)

The challenges of keeping the sensing margin of BLSA sufficiently large are mainly due to several reasons. First, the cell capacitance becomes smaller due to scaling and the reduction in cell signal further suppresses the ΔV signal, making it even harder to detect. Second, transistors threshold voltage mismatch caused by process, voltage and temperature (PVT) variation introduces an intrinsic offset that can bias

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the BLSA toward one state (Moon & Chung, 2010). Finally, coupling noise from adjacent bit-lines, especially in high density arrays, further interrupt the sensing signal (Kim et al., 2019). When the combined effect of offset and noise becomes larger than the real ΔV signal, the BLSA will fail to latch correctly, leading to read errors. (Choe, 2021; Kim et al., 2025)

For the remaining sections, this paper is organized as follows: Section 2 provides a detailed review of conventional BLSA operations and evaluates the limitations of current state-of-the-art offset compensation (OC) techniques. Section 3 introduces the novel HDOC architecture and its operational phases. Post-layout simulation results and performance benchmarks are discussed and analyzed in Section 4, followed by concluding remarks and future directions in Section 5.

2. Methodology

2.1. The sensing failure mechanism in conventional BLSAs

Conventional BLSA operation follows a typical sequence: precharge (PRE), charge sharing (CS), and main sensing (MS). In an ideal scenario, the BLSA triggers when the bit-line differential, ΔV is non-zero. However, the VTH mismatch between cross-coupled inverter pairs creates an offset voltage that is indistinguishable from the cell signal. If the cell signal, ΔV detected by the BLSA is smaller than the offset voltage, V_{OS}, or if they have opposite polarities, the BLSA fails to latch the correct value (‘0’ or ‘1’), causing functional failure.

2.2. Prior offset-cancellation (OC) techniques

To address the sensing margin issues, various offset cancellation (OC) techniques have been proposed. They can be categorized into four main categories: inverter short (Cheng, 2025; Lim et al., 2025; Liu et al., 2024; Moon & Chung, 2010), diode connection (Kang, 2015; Kim et al., 2018; Kim et al., 2019; Nam et al., 2025), current mirror (Huang et al., 2022; Sang Hoon et al., 2002; Sanghoon et al., 2002), or using coupling capacitors to store and isolate the offset from the main bit-lines during the sensing phase (Jeon & Chae, 2025; Jung et al., 2023; Yoon et al., 2020).

The first category, the inverter-short or "flip-point" method, shorts the input and output of the BLSA inverters to bias the nodes at their switching threshold (Moon & Chung, 2010). While this provides high sensitivity, it creates a direct path from VDD to ground, resulting in significant short-circuit power overhead and making the circuit highly susceptible to power supply noise during calibration (Liu et al., 2024). Similarly, current-mirror-based OC adjusts the bit-line voltage to equalize the currents flowing through the latch transistors (Sanghoon et al., 2002). However, these schemes suffer from high static power consumption because the transistors must be biased in the saturation region during the OC phase to achieve effective compensation (Lim et al., 2025).

To address the area and power constraints of the aforementioned methods, diode-connection-based offset compensation (such as OCSA (Kang, 2015) and BRV-SA (Kim et al., 2019)) has been proposed. These designs configure latch transistors as diodes to sample V_{TH} directly onto the bit-lines or internal nodes during the OC phase. Although this method is highly area-efficient, it typically still requires a dedicated OC phase that must be completed before charge-sharing begins, thereby increasing the total row cycle time (Lim et al., 2025). Furthermore, as the bit-lines are often biased away from the equalization voltage (V_{EQ}) to store the captured offset, these designs frequently suffer from an Imbalanced Sensing Margin (ISM), where the sensing margins for data ‘0’ and data ‘1’ become asymmetrical (Nam et al., 2025).

Alternatively, capacitive-coupling (CC) based techniques (such as COSA (Yoon et al., 2020) and FPOSA (Liu et al., 2024)) employ capacitors to store the offset voltage while maintaining the bit-lines at V_{EQ}. While these methods are effective at reducing decision threshold variations and preventing ISM, standard CC architectures often introduce significant area overhead due to the large silicon footprint of the capacitors and can increase sensitivity to ambient coupling noise. More recent published works, such as the DISA (Lim et al., 2025), HB-COSA(Jung et al., 2023) and HCP-COSA (Jeon & Chae, 2025), attempt to resolve the timing penalty by enabling simultaneous OC and charge-sharing; however, the complexity of managing stacked inverter architectures remains a significant implementation challenge.

Despite these advancements, a clear research gap exists for a solution that simultaneously achieves low-voltage, high-speed operation, and sensing symmetry. Current literature extensively explores trip-point and current-mirror hybrids (Cheng, 2025; Huang et al., 2022), yet there is limited study on the integration of diode-connection mechanisms with capacitive coupling. The methodology proposed in this work bridges this gap by utilizing isolation switches and capacitive coupling to "hide" the diode-based offset cancellation phase within the existing charge-sharing window. This approach ensures that the bit-lines remain at V_{EQ} to prevent ISM and mitigate coupling noise, providing a robust, high-speed sensing solution without the timing penalties.

3. Proposed work

3.1. Circuit and operation

The proposed work introduces a **Hidden Diode-Connected Offset Cancellation (HDOC)** sense amplifier that combines and extends the key advantages of prior architectures into a single low-overhead sensing framework. Similar to OCSA (Kang, 2015), it employs a diode-connected NMOS latch during the offset-cancellation phase to sample and store the threshold-voltage mismatch on the bit-lines without requiring additional calibration circuitry. In addition, a capacitive coupling mechanism is used to store the offset voltage relative to the equalized bit-line voltage (equals to $V_{offset} - V_{EQ}$), enabling accurate offset tracking while maintaining balanced sensing conditions. Inspired by BRV-SA (Kim et al., 2019), the stored offset is further reused to provide a hidden boosting effect that enhances the sensing ΔV prior to regeneration, improving noise immunity and accelerating the latching process under low-voltage operation. Overall, HDOC achieves integrated offset cancellation and dynamic signal enhancement with improved sensing margin and reduced failure rate. The circuit schematic of the proposed work is illustrated in **Fig. 1**, which consists of 12 transistors and 2 capacitors (12T + 2C).

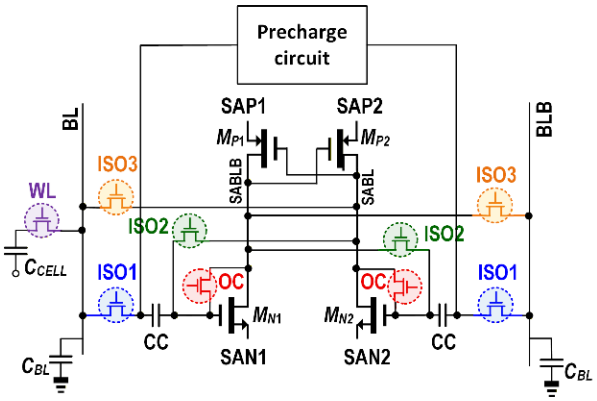


Fig. 1 Proposed HDOC architecture schematic diagram.

Precharge Phase: During the initial precharge stage, the control signals **PRE**, **ISO1**, and **ISO2** are driven high, which activates the precharge circuitry and all isolation transistors. This configuration establishes a low-impedance path that equalizes both the external bit-lines (BL and BLB) and the internal sensing nodes to the equalization voltage level, V_{EQ}, typically defined as VDD/2. By ensuring all nodes are biased at a common reference point, the architecture eliminates any residual charges from previous cycles, preparing the system for high-precision offset sampling.

Hidden Offset Cancellation and Charge Sharing Phase (OC & CS): In this phase, the **OC** signal is asserted to configure the NMOS latch transistors into a diode-connected state, while the BLSA power supplies, **SAP1/2** and **SAN1/2**, are activated to VDD and VSS respectively. Simultaneously, the bit-line is temporarily separated from the coupling capacitor to perform charge sharing with the memory cell. While the bit-line voltage develops based on the cell signal, the internal end of the coupling capacitor is charged toward V_{EQ} as the latch transistors sample their unique threshold voltage V_{TH} mismatch. This mechanism allows the captured offset to be stored directly across the capacitors while simultaneously performing charge sharing. Because the **PRE** signal remains high, the bit-line voltage maintains its centered reference level, $\mathbf{V_{EQ}}$, while the internal nodes sample the unique threshold voltage V_{TH} mismatch of the latch transistors. The captured offset is stored directly across the coupling capacitors, effectively "hiding" the cancellation period within the standard charge-sharing window to shorten the row cycle time.

Pre-sensing and Boosted Reference Voltage (PS & Boost): Transitioning to the pre-sensing phase, **ISO1** is driven high to allow the accumulated signals at **BL** and **BLB** to be transferred to the gates of the latch transistors through the coupling capacitors. Since the capacitors have already captured the V_{TH} mismatch, the contribution of the threshold-voltage mismatch to the effective sensing differential is reduced, allowing the cell-induced ΔV to be amplified more effectively. To further enhance the sensing margin, a voltage boosting mechanism is applied by selectively activating an inverter to reversely amplify the reference level. This process significantly widens the voltage difference between the internal nodes before the final latching process begins, ensuring high-speed reliability even at low supply voltages.

Main Sensing Phase: The final operation is the main sensing phase, where **ISO2** is HIGH to engage the full cross-coupled feedback loop of the amplifier. With the complete activation of **SAP1** and **SAN1**, the circuit enters a regenerative state where the pre-amplified differential signal is rapidly driven to full-rail CMOS levels. The isolation switches ensure that **BL** and **BLB** accurately track the internal nodes, resulting in the bit-lines latching to the correct logic value. Because the bit-lines were maintained at $\mathbf{V_{EQ}}$ during the critical sampling stages, the resulting sensing margin remains perfectly symmetrical, effectively eliminating the Imbalanced Sensing Margin (ISM) issues common in conventional offset-compensated designs.

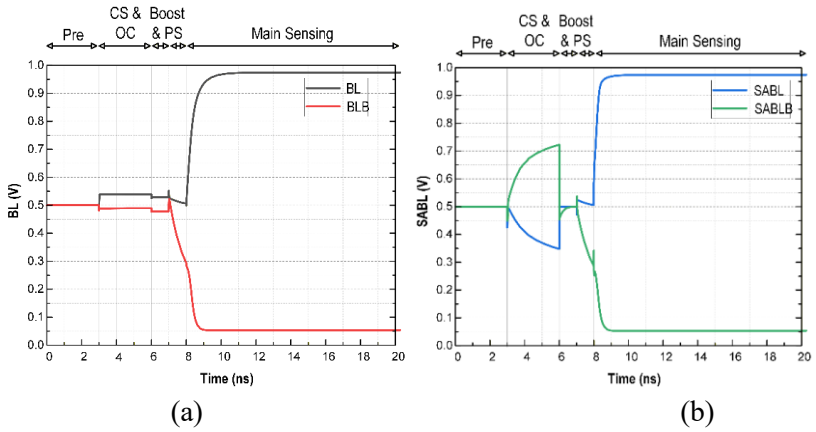


Fig. 2 Transient waveforms for (a) BL and BLB, and (b) SA_BL and SA_BLB when reading D1.

Fig. 2 illustrates the transient waveforms of reading data '1' (D1) operation. During the precharge phase, BL, BLB, SA_BL and SA_BLB are initialized close to the equalization voltage, V_{EQ}. During the CS & OC phase, the external bit-lines (BL and BLB) remain approximately centered around V_{EQ}, while internal sensing nodes (SA_BL and SA_BLB) develop a voltage difference associated with threshold-voltage mismatch. During the subsequent Boost & PS phase, the stored offset is used to establish a larger initial differential at the internal sensing nodes. Once main sensing is enabled, this pre-established differential is rapidly amplified by the cross-coupled latch, causing SA_BL and SA_BLB to approach the supply rails. The corresponding BL and BLB waveforms show the same regenerative behavior, with BL reaching a high logic level and BLB being pulled toward ground for the D1 operation. The transition from the pre-sensing state to full regeneration occurs at approximately 8 ns.

4. Simulation result and discussion

Post-layout simulations were performed using same length 60nm for all transistors, while the width ratio of PMOS and NMOS is set to 3:1, and the other control switches use a minimum width of 200nm. Utilizing a 65nm CMOS technology, the design's reliability against process variations and transistor mismatch was verified using 100 Monte Carlo simulation samples. The simulation environment utilized a fixed cell capacitance C_{cell} of 8 fF, while the supply voltage VDD varied from 0.80 V to 1.0 V. Additionally, the C_{BL}/C_{cell} ratio was swept across values of 4, 8, and 10 to evaluate the design's performance under various bit-line loading conditions. The following analysis and discussion focus on the **'Read D1'** operation to validate the design's offset compensation and boosting capabilities.

4.1. Sensing speed

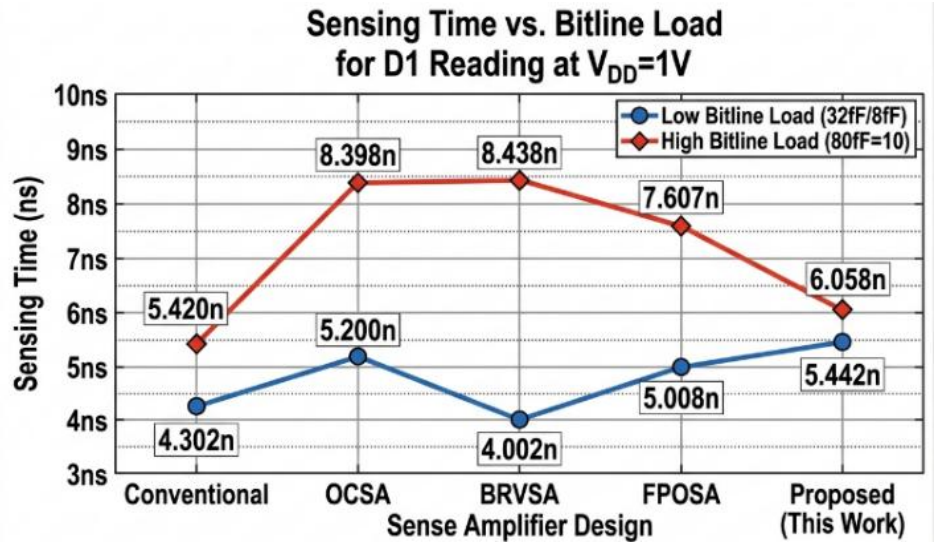


Fig. 3 Comparison of sensing speed across different bit-line loading (CBL/Ccell ratio = 4 and 10).

Sensing speed is defined as the transient delay from the start of ACTIVE command until the differential voltage between the bit-lines (ΔV) is fully amplified to its respective supply rails. (Huang et al., 2022; Kim et al., 2019; Li et al., 2023; Liu et al., 2024) To evaluate the impact of bit-line loading on performance, Fig. 3 compares the sensing times of the HDOC against prior works during a 'D1' operation. The comparison is conducted under two different loading conditions: a light load of C_{BL}/C_{cell} = 4 and a high-density load of C_{BL}/C_{cell} = 10.

As expected, all designs experience an increase in sensing time when the bit-line capacitance goes up, because heavier loads naturally slow down the cell signal amplification. However, the proposed work shows the lowest sensitivity to the variations in load capacitance. When the loading ratio increases from 4 to 10, the sensing delay of the proposed design only increases by 11.3%. In comparison, prior architectures experience much more drastic performance drops. The sensing delays for OCSA, BRVSA, and FPOSA spike by 47.9%, 59.9%, and 48.5% respectively. Even the conventional SA slows down by 26.0%. This demonstrates that HDOC offers much better stability and robustness when subjected to high-density bit-line loading conditions.

4.2. Sensing yields

Sensing yield is defined as the probability of a valid data output across the total number of simulated Monte Carlo samples (100 samples are used), expressed as Eq.1:

$$Sensing\ Yield\ = \frac{number\ of\ corect\ samples}{total\ number\ of\ samples} * 100 \tag{1}$$

A critical metric governing this yield is the tRCD (RAS-to-CAS delay), which defines the available time for the bit-lines to develop a sufficient differential voltage. (Jung et al., 2023) To align with modern DRAM operating conditions, a strict 15-ns sensing window is enforced. Consequently, in the yield

calculations, a sensing operation is only considered successful if the signal amplifies to at least 80% of VDD without bit-flipping strictly within this 15 ns window. If the bit-lines fail to reach this voltage threshold or experience a late data inversion after the time limit, the cycle is counted as a sensing failure, which will directly lower the overall yield.

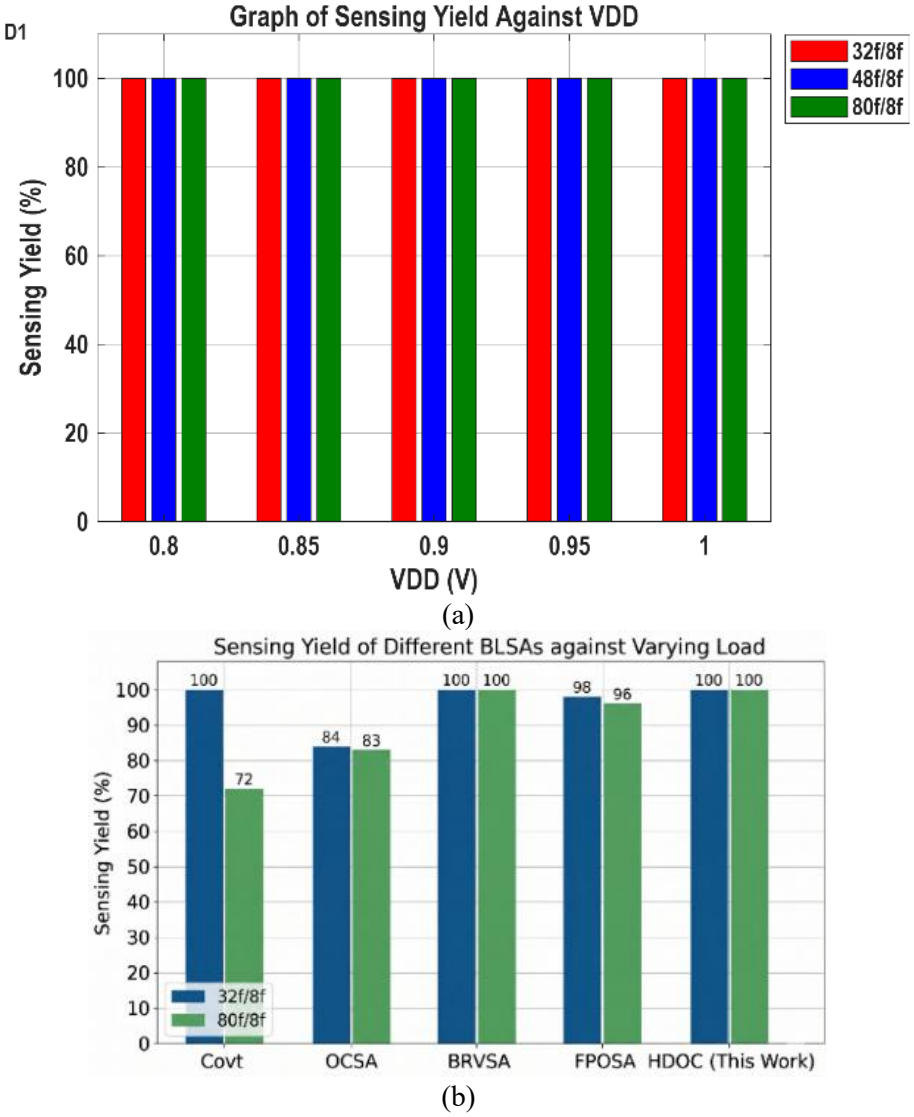


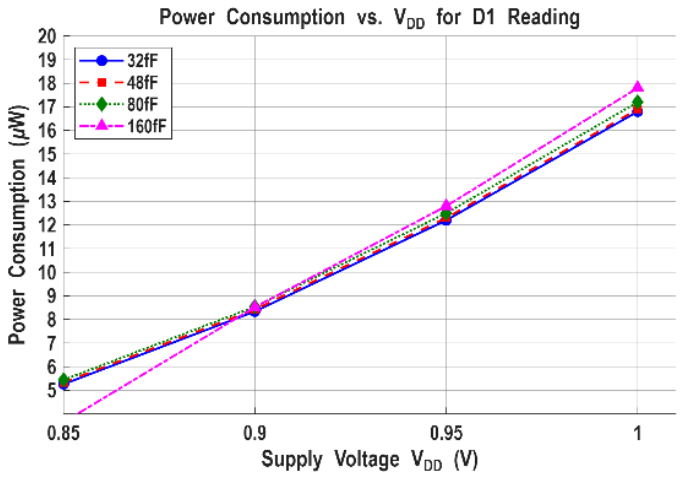
Fig. 4 Comparison of sensing yield under varying (a) VDD (0.8 to 1.0V) and (b) bit-line capacitance loads (CBL/Ccell ratio = 4,8,10).

Fig. 4(a) depicts the sensing yield of the proposed HDOC as a function of the supply voltage VDD across diverse bit-line loading conditions C_{BL}/C_{cell}. The post-layout simulation results demonstrate that the proposed design maintains a 100% sensing yield across a wide supply voltage range from 0.80 V to 0.95 V for bit-line capacitance ratios up to 10. Even at the highest voltage of 1.0 V, the proposed design still achieves 100% yield under both the standard and heavy load of C_{BL}/C_{cell} = 4 and 10.

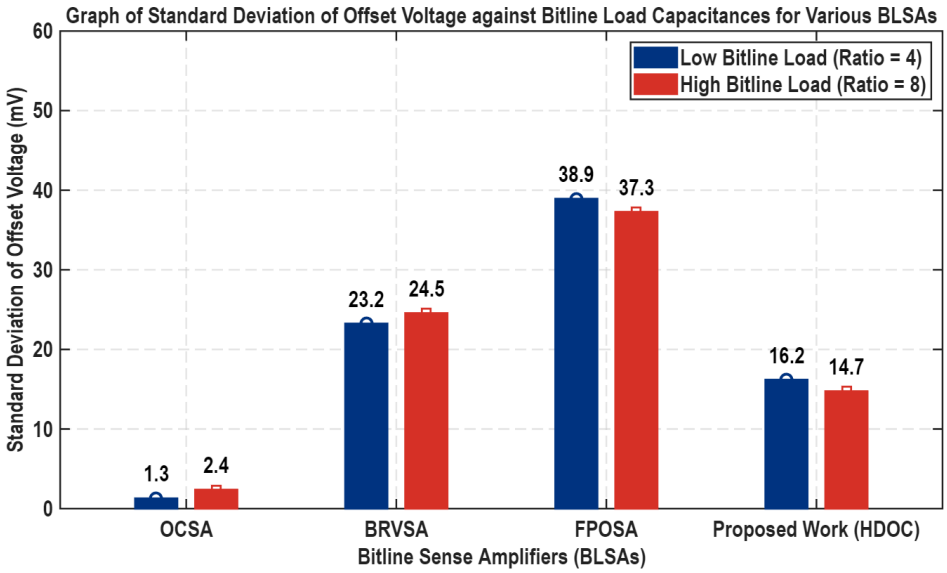
The advantages of the proposed HDOC SA over existing architectures are illustrated in the comparative analysis presented in Fig. 4(b). When the capacitance loading ratio increases, prior works suffer from

yield degradation up to 28%. Conversely, the proposed HDOC SA delivers an uncompromised 100% sensing yield under both conditions. Furthermore, post-layout simulations also yield a 100% sensing yield across all process corners (tt, ff, ss, sf, fs), indicating its stability and reliability. These results substantiate that the proposed architectural modifications successfully mitigate local transistor mismatch and parasitic loading effects, offering better stability and design margin compared to state-of-the-art designs.

4.3. Average power consumption



(a)



(b)

Fig. 5 Comparison of power consumption under varied (a) power supply and (b) bit-line load capacitances.

In this simulation, the average power consumption P_{avg} is determined by multiplying the supply voltage, VDD by the time integral of the transient current obtained from the circuit simulations (Lim et al., 2025; Liu et al., 2024). The calculation is expressed as Eq. 2:

$$P_{avg} = \frac{1}{t2 - t1} \int_{t1}^{t2} VDD(t) * I(t)\, dt \tag{2}$$

where VDD(t) is the transient supply voltage and I(t) is the total transient current drawn from the power supply terminal.

Referring to the graph in **Fig. 5**(a), the power consumption of the proposed design is highly dependent on the supply voltage. When VDD scales up from 0.80 V to 1.0 V, the average power consumption naturally increases across all test cases due to the higher operating voltage. However, varying the bit-line capacitance C_{BL} from 32 fF up to 80 fF has only slight impact on the overall power consumption profile. The data lines for all four loading conditions are tightly bundled together across the entire voltage sweep, proving that the proposed architecture successfully minimizes any unnecessary dynamic power overhead when driving heavy bit-line loads.

Fig. 5(b) highlights the average power consumption derived from 100 Monte Carlo simulation runs, comparing the proposed work against existing architectures at VDD = 1.0V. While the conventional design consumes the least power (at the cost of the severe yield drops discussed earlier), the proposed design provides high sensing yield with moderate power consumption. The proposed design maintains low power consumption compared to the high-performing FPOSA which also uses capacitive coupling hybrid topology. Under high bit-line loading C_{BL}/C_{cell} = 10, the proposed work consumes only 17.21uW compared to FPOSA's 40.73uW, achieving a significant **power reduction of over 57.7%**. This proves that the proposed architecture delivers better stability and mismatch compensation without introducing too much power overhead.

4.4. Offset voltage against Process, Voltage and Temperature (PVT) variations

Fig. 6 shows the standard deviation of the offset voltage across wide temperature range (-10, 27, 85°C) during two different operations, D0 and D1 sensing at high load C_{BL}/C_{cell} = 8. Despite drastic temperature change, the fluctuation of offset voltage was small, showing that the proposed work is highly robust against thermal variations. The overall comparison is summarized in the **Table 1**.

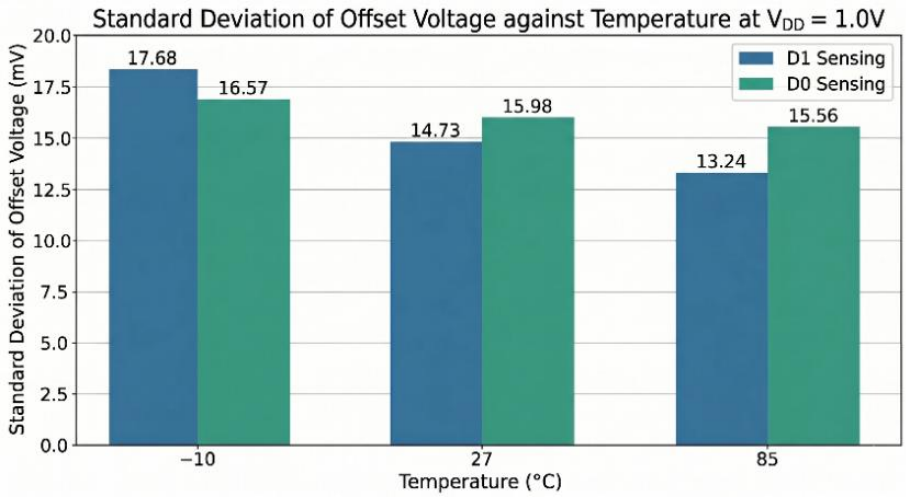


Fig. 6 Standard deviation of offset voltage under various temperature (-10, 27 and 85°C).

Table 1. Comparison of BLSAs with this work for D1 sensing.

	Conventional BLSA	FPOSA	BRVSA	OCSA	This work
OC method	Without OC	Trip-point + CC	Diode-connected	Diode-connected	Diode-connected + CC
Area	6T	13T+1C	8T	8T	12T+2C
σ of Offset Voltage (mV)	N/A	37.27*	24.54*	2.361*	14.73#
Power (uW)	2.401*	40.73*	12.74*	10.41*	17.21#
Sensing Speed (ns)	5.42*	7.607*	8.438*	8.398*	6.058#
Sensing Yield (%)	72*	96*	100*	83*	100#

*Based on 65nm technology node, pre-simulation result with CBL/Ccell = 80f/8f and VDD =1.0V.
Post-layout simulation results.

5. Conclusion

In conclusion, this work presents a robust, low-voltage DRAM bit-line sense amplifier architecture designed to overcome the severe scaling limitations of device mismatch and parasitic bit-line loading. By decoupling the offset calibration mechanism from the bit-line capacitance, the proposed design achieves a 100% sensing yield across a wide operating envelope, spanning extreme process corners, temperatures from -10°C to 85°C, and supply voltages VDD ranging from 0.8 to 1.0V. Post-layout simulations show that the proposed design maintains a low offset-voltage variation while achieving competitive power consumption. While this takes slightly longer to sense under normal conditions, it is actually the fastest design at high capacitive loads because it has the lowest sensitivity to high bit-line capacitance. Future work may focus on evaluating the architecture in more advanced technology nodes, such as sub-20-nm processes, to further assess its scalability. In addition, silicon fabrication and measurement would provide experimental validation of the proposed architecture and enable a more comprehensive evaluation of its practical performance. Nonetheless, these improvements prove that the proposed offset-compensation technique is a highly scalable, energy-efficient, and reliable solution for next-generation, high-density DRAM systems.

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